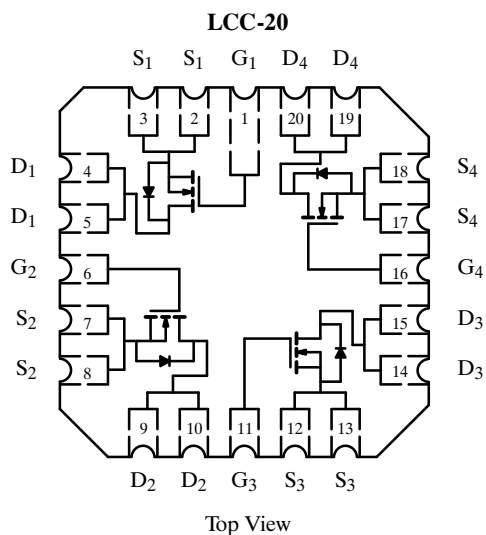


### Quad N-Channel Enhancement-Mode MOSFET

#### Product Summary

V <sub>DS</sub> (V)	r <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)
20	0.1 @ V <sub>GS</sub> = 10 V	5
	0.2 @ V <sub>GS</sub> = 4.5 V	1



#### Absolute Maximum Ratings (T<sub>A</sub> = 25°C Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	20	V
Gate-Source Voltage	V <sub>GS</sub>	±20	
Continuous Drain Current <sup>a</sup>	I <sub>D</sub>	T <sub>A</sub> = 25°C	5
		T <sub>A</sub> = 100°C	3
Pulsed Drain Current <sup>a</sup>	I <sub>DM</sub>	14	A
Continuous Source Current (Diode Conduction)	I <sub>S</sub>	3	
Maximum Power Dissipation	P <sub>D</sub>	T <sub>A</sub> = 25°C	3
		T <sub>A</sub> = 100°C	1.3
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 150	°C

#### Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Case	R <sub>thJC</sub>	40	°C/W

Notes:

a. Drain current limited by package construction.

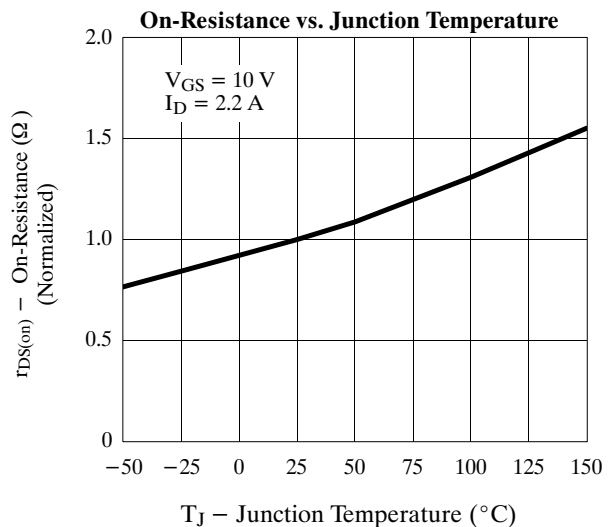
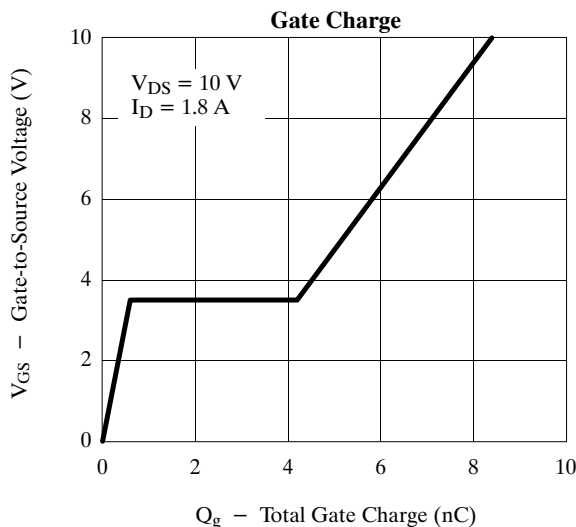
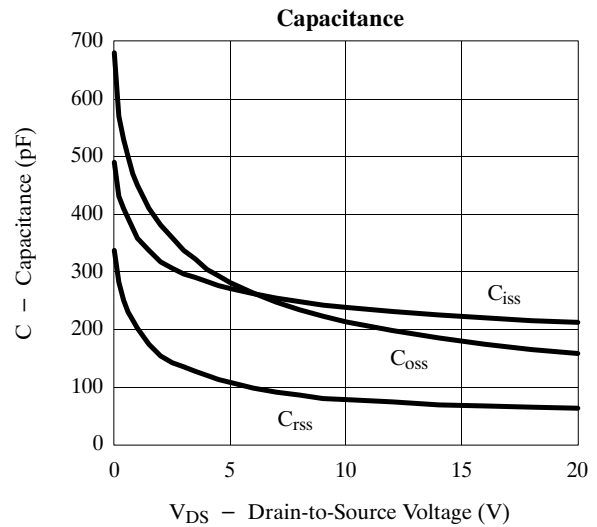
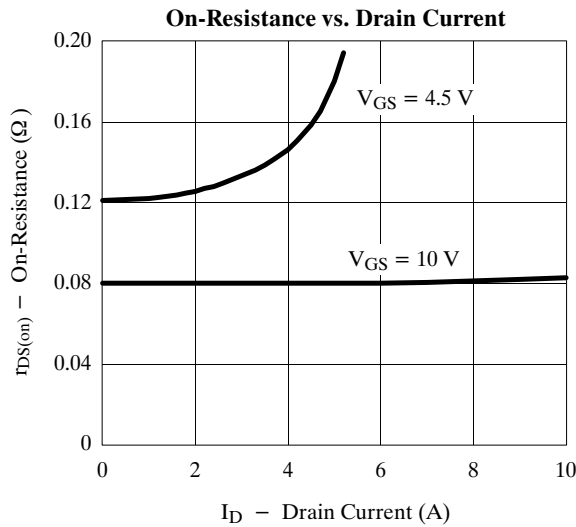
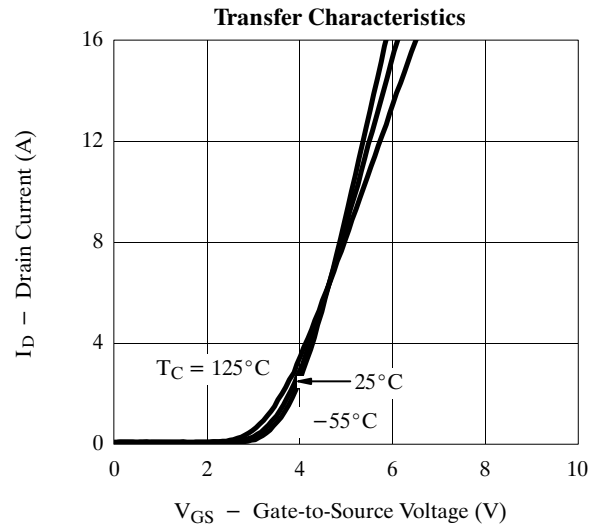
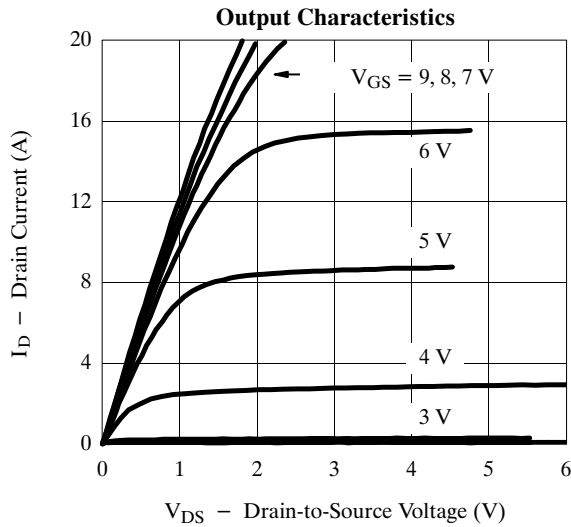
### Specifications ( $T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Max	Unit
<b>Static</b>					
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	20		V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1	3.5	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$		$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 16\text{ V}, V_{GS} = 0\text{ V}$		10	$\mu\text{A}$
		$V_{DS} = 16\text{ V}, V_{GS} = 0\text{ V}, T_J = 125^\circ\text{C}$		25	
On-State Drain Current <sup>b</sup>	$I_{D(on)}$	$V_{DS} = 10\text{ V}, V_{GS} = 10\text{ V}$	7		A
Drain-Source On-State Resistance <sup>b</sup>	$r_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 3\text{ A}$		0.1	$\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 1\text{ A}$		0.2	
Forward Transconductance <sup>b</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}, I_D = 3\text{ A}$	2		S
<b>Dynamic</b>					
Input Capacitance <sup>a</sup>	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 16\text{ V}, f = 1\text{ MHz}$		500	nC
Output Capacitance <sup>a</sup>	$C_{oss}$			300	
Reverse Transfer Capacitance <sup>a</sup>	$C_{rss}$			125	
Total Gate Charge <sup>a, c</sup>	$Q_g$	$V_{DS} = 10\text{ V}, V_{GS} = 10\text{ V}, I_D = 5\text{ A}$		30	
Gate-Source Charge <sup>a, c</sup>	$Q_{gs}$			5	
Gate-Drain Charge <sup>a, c</sup>	$Q_{gd}$			8	
Turn-On Delay Time <sup>c</sup>	$t_{d(on)}$		$V_{DD} = 10\text{ V}, R_L = 2\ \Omega$ $I_D \cong 3\text{ A}, V_{GEN} = 10\text{ V}, R_G = 6\ \Omega$		30
Rise Time <sup>c</sup>	$t_r$			35	
Turn-Off Delay Time <sup>c</sup>	$t_{d(off)}$			70	
Fall Time <sup>c</sup>	$t_f$			30	
<b>Source-Drain Diode (<math>T_C = 25^\circ\text{C}</math>)</b>					
Pulsed Current	$I_{SM}$			3	A
Diode Forward Voltage <sup>b</sup>	$V_{SD}$	$I_F = 3\text{ A}, V_{GS} = 0\text{ V}$		1.6	V
Reverse Recovery Time	$t_{rr}$	$I_F = 3\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		100	ns

Notes:

- Guaranteed by design, not subject to production testing.
- Pulse test; pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .
- Independent of operating temperature.

## Typical Characteristics (25°C Unless Otherwise Noted)



## Si8956AZ/883

### Typical Characteristics (25°C Unless Otherwise Noted)

